2011 International Symposia on

Extreme Ultraviolet Lithography and Lithography Extensions

October 17-19 and October 20-21 • Miami, Florida

EUV Readiness and EUV PPT Performance

Han-Ku Cho

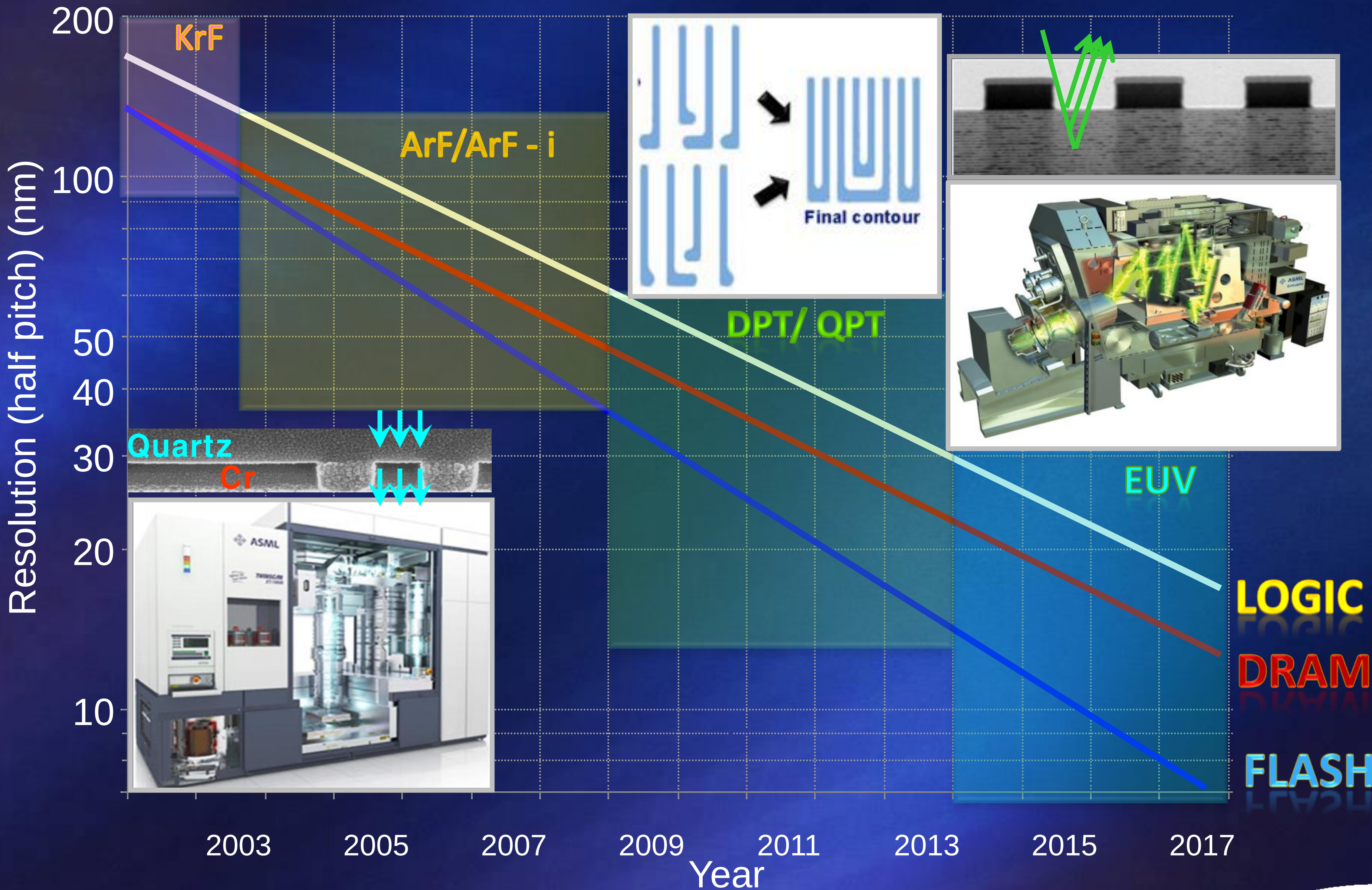
SAMSUNG Electronics

SAMSUNG

Contents

- ❑ Introduction
- ❑ EUV PPT performance and its challenges
- ❑ Resist readiness and issues
- ❑ Mask readiness and issues
- ❑ Conclusions

Evolution of litho technology



Current status of litho candidate

- ❑ **Nano Imprint**
  - ✓ S-FIL* meets several key ITRS requirements for 22nm node HVM
  - ✓ Key obstacle
    - Defectivity (~ 100 def/cm^2 → target : 0.1 def /cm^2)
    - Overlay (~ 15nm for MMO → target : 5nm for MMO)
    - Throughput(~ 4wph → target : 20wph)
- ❑ **ML2 (Mask-less Lithography)**
  - ✓ Two main technologies (MAPPER and REBL) still do not show 10wph
  - ✓ Key obstacle: Low throughput from the sequential exposure of pixels
- ❑ **DPT/QPT**
  - ✓ Low mask cost and process stability
  - ✓ Cost from added process steps and layers
  - ✓ Lack of design flexibility

* S-FIL : Step & Flash Imprint Lithography

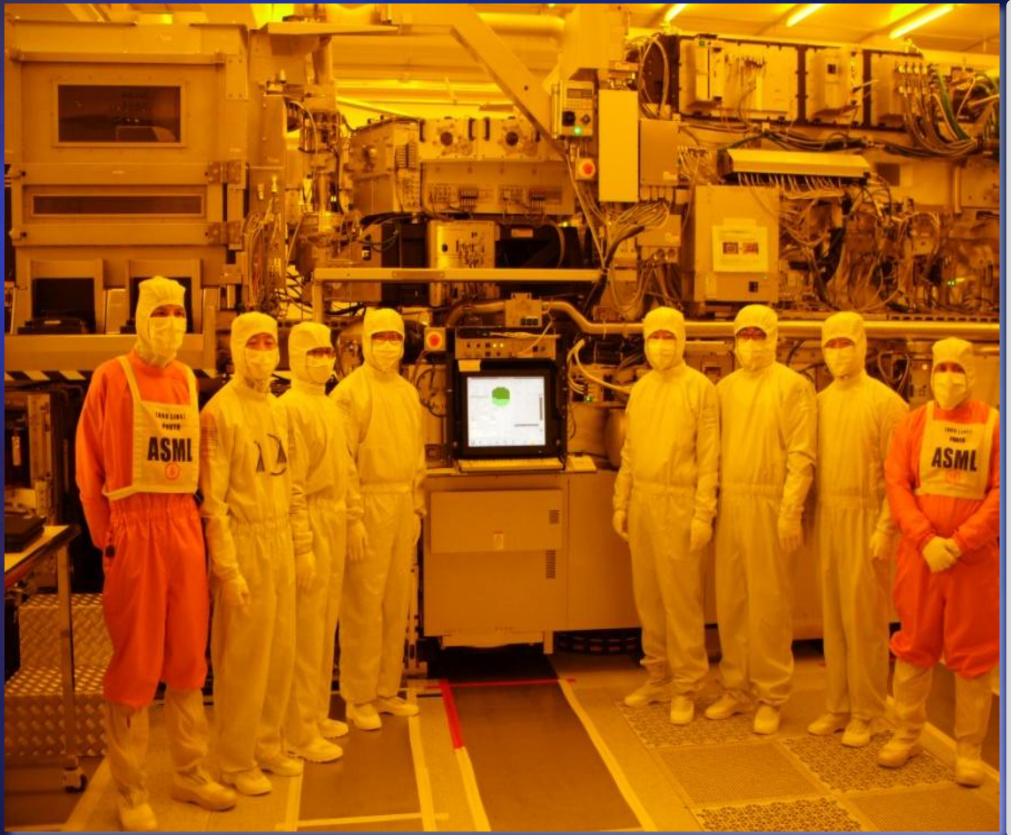
SAMSUNG

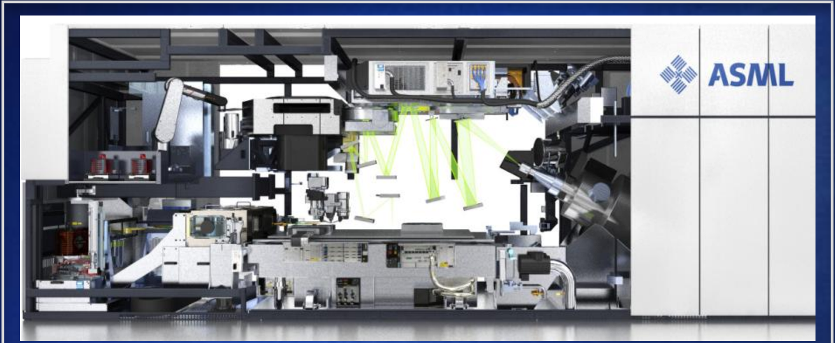
Contents

SAMSUNG

EUVL has been started for DRAM development

- NXE:3100 @ Samsung (Dec./2010)
  - ✓ Worldwide 1st EUVL scanner for pilot line (pre-production tool)





Wavelength	13.5 nm
NA	0.25
Source	LPP
# of PO mirrors	6
Field size	26 x 33 mm^2
Magnification	4x reduction
Sigma	0.8
CRA @Mask	6 degrees
Flare	< 6%

Installation of NXE:3100 (Dec 2010)

- Full installation taken ~ 90 days
  - ✓ Used 3 floors and big area for parts stock

3rd — Scanner/ Source

2nd — CO_2 laser / Controls

1st — Facilities(Pre Vac.)

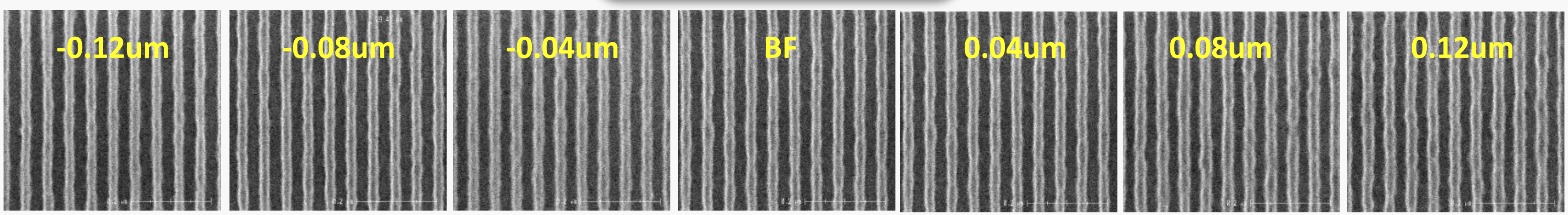
NXE:3100 SAT (Feb 2011)

	Specification	Results
Resolution	27nm	
NA / σ	0.25 / 0.8	
Overlay (DCO/MMO)	DCO < 4nm MMO < 7nm	
Throughput (Dose)	60 wph ($10mJ/cm^2$)	
Source power	100W	

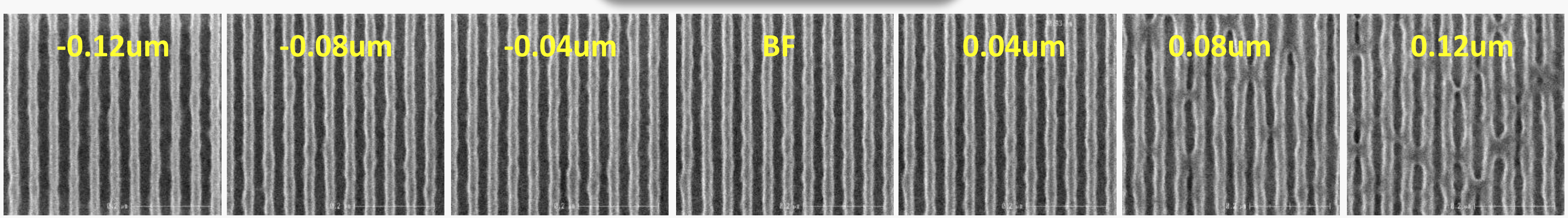
Resolution

- NXE:3100 resolution and DOF (Dec. 2010)
  - ✓ NA=0.25, Conv, resist dose ~ 10mJ/cm^2
  - ✓ 25nm HP resolution is achieved with SEVR-140
  - ✓ DOF ~200nm is achieved at 27nm HP

27nm L/S



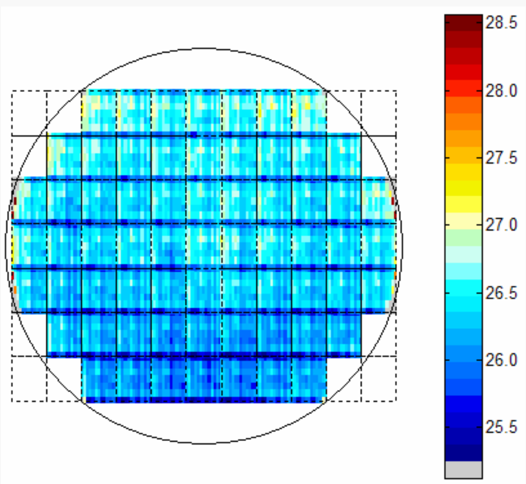
25nm L/S



CD uniformity

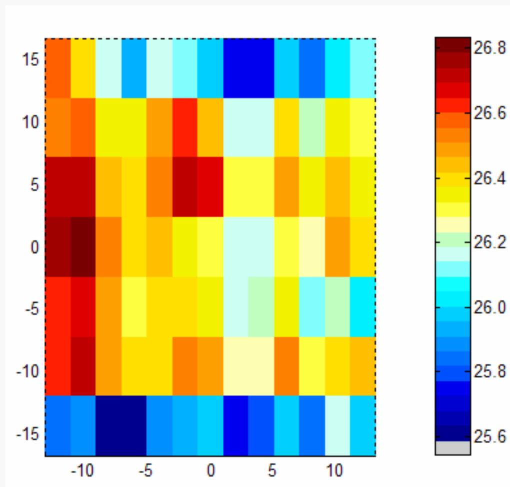
- Full wafer 27nm dense L/S
  - ✓ Measured data without correction
  - ✓ No dose stability issue observed

Full wafer



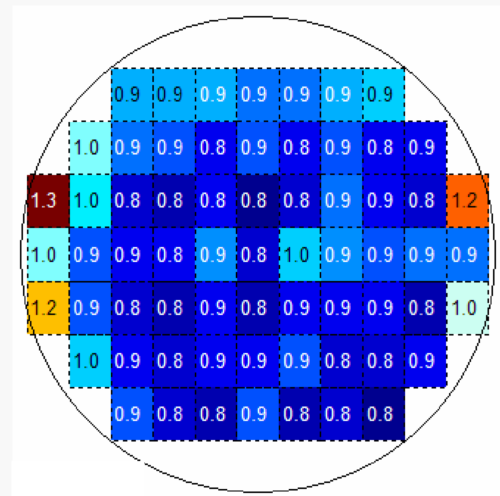
Mean CD = 26.3nm,
CDU = 1.0nm

Intra Field



Mean = 26.3nm,
Avg. CDU = 0.8nm (3σ)

Inter Field



All fields < 1.3nm (3σ)

Overlay Performance (MMO)

- Localized grid distortion can be compensated with an revised calibration step (optimization of calibration SW)
- Further grid/lens distortion correction to achieve R&D requirements
  - ✓ Increase correction order/parameter

Spring, 2011

Grid calibration improvement

Summer, 2011

SAMSUNG

Throughput / source power

- Required source power > 100W (equivalent to 60wph)
- Current power < 10W

Major challenges of NXE:3100

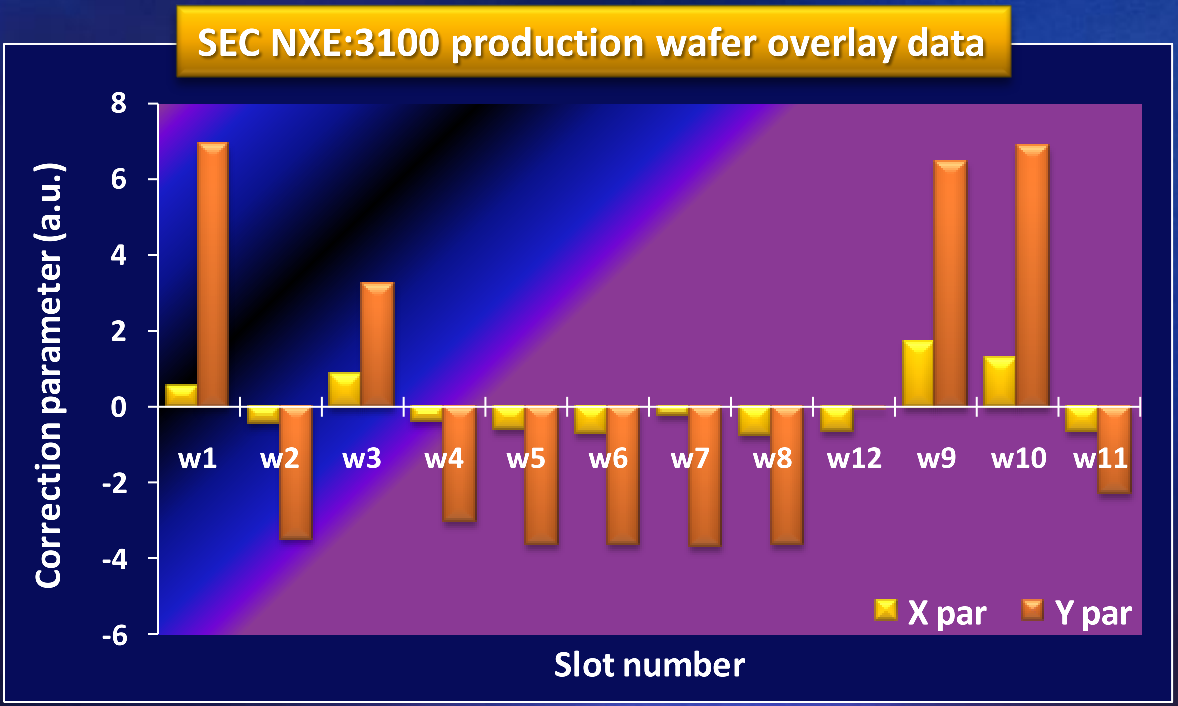
- Lower productivity
- Overlay drift / variation
- Reticle front side/back side contamination

Lower productivity

- ❑ Source power and productivity are on the highest risk

Overlay instability

- **Scanner stability not confirmed**
  - ✓ Overlay correction parameter variation in batch
  - ✓ Scanner thermal behavior + Low throughput
  - ✓ Long term stability of in-field & grid fingerprint should be confirmed
  - ✓ SW correction test on-going, system stability monitoring test planned

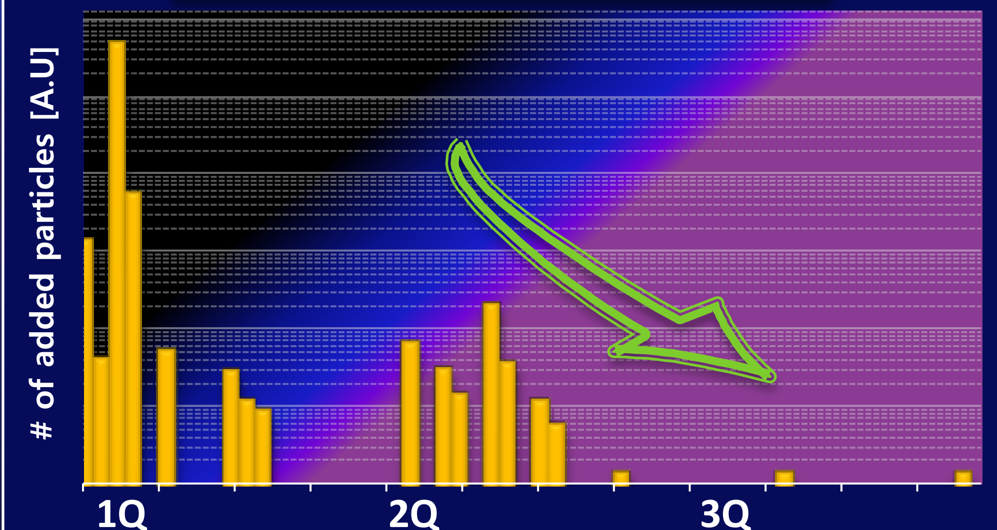


SAMSUNG

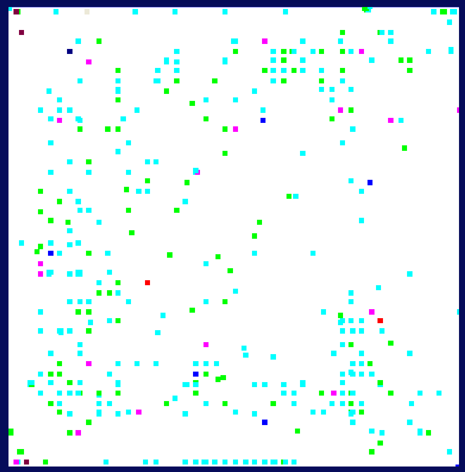
Reticle contamination

- Reticle contamination (Front side/ back side)
  - ✓ It is important to improve not only molecular contamination, but also system-induced particles
  - ✓ Improvement of reducing system-induced particles is in progress
  - ✓ Cleanliness management of the system should be confirmed
  - ✓ Clean clamp, pod and reticle are all needed to maintain acceptable defectivity in production

Front side



Back side



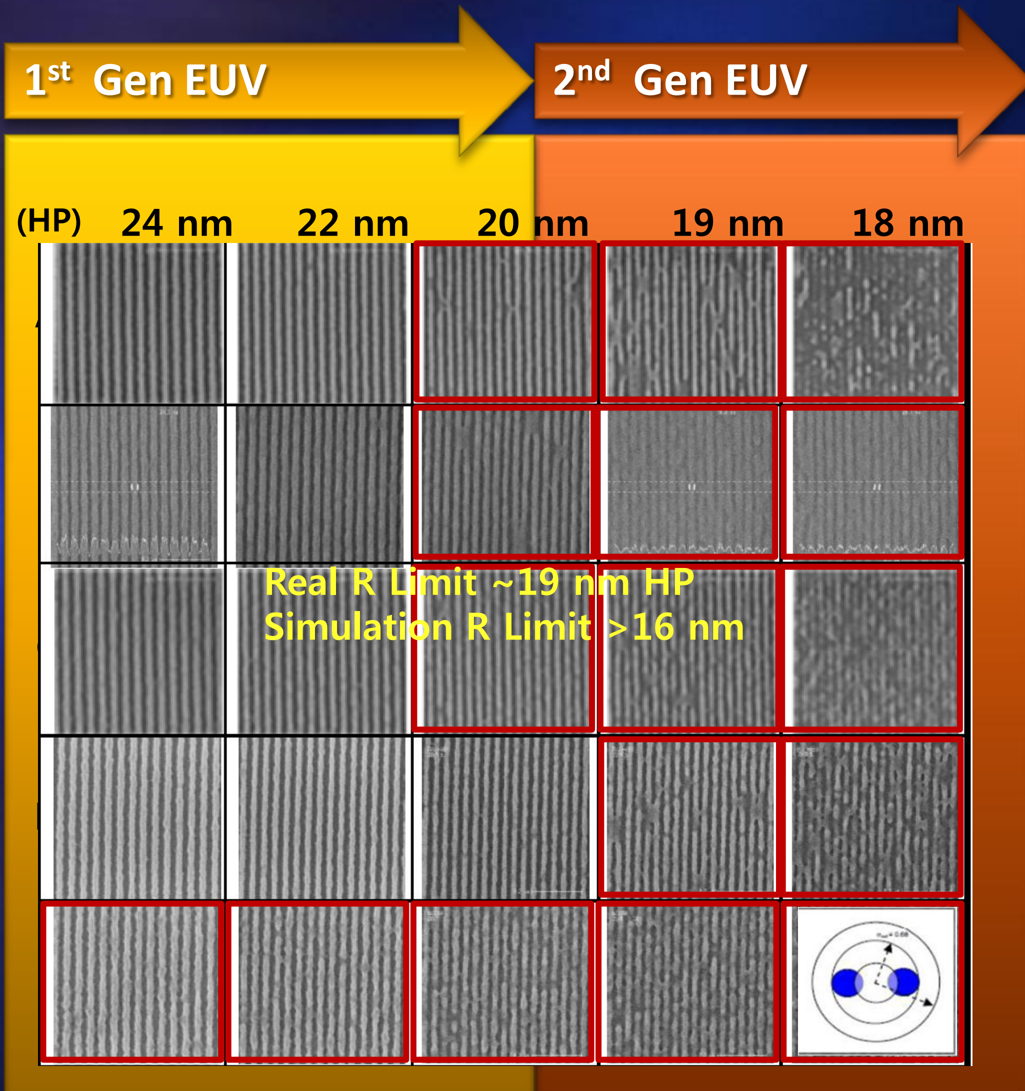
Several hundreds of #

SAMSUNG

Contents

SAMSUNG

EUV resist classification @Samsung



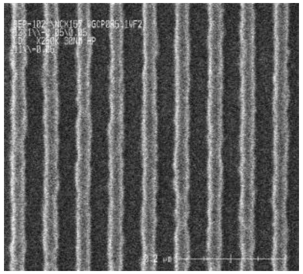
- 20nm HP resolution is hardly achieved with a condition capable of 16nm HP resolution (@ Albany MET with dipole)
- Alternative resist is required and called as 2nd generation EUV resist.

SAMSUNG

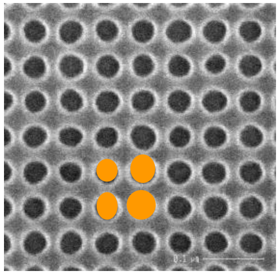
Critical issues for 1st generation EUV

Issue 1

Local CD variation (LWR & LCDU)



LWR@30nm HP

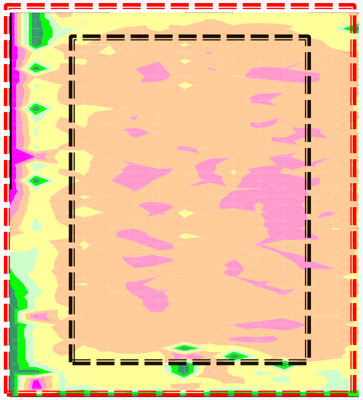


Local CDU@30nm HP

796916, Vol.7969, SPIE 2011

Issue 2

CD variation across a field @ ADT



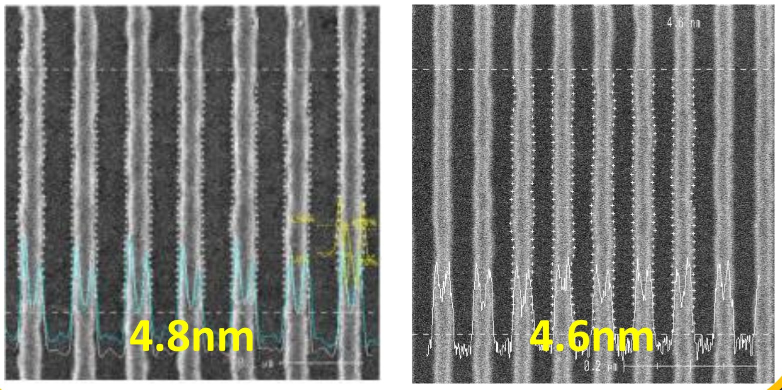
796918, Vol.7969, SPIE 2011

Issue 1: LWR improvement

Resist A

After Litho

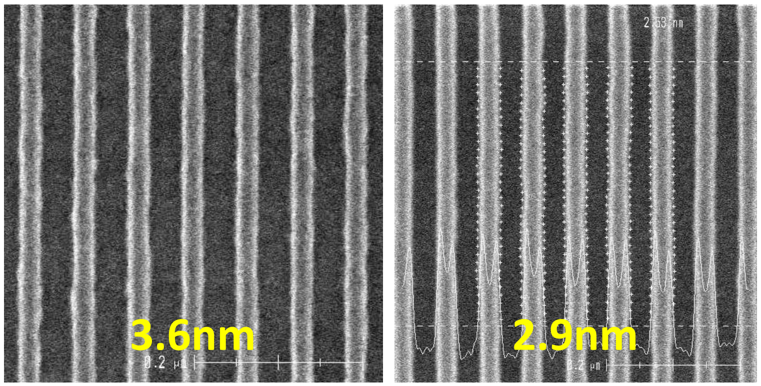
After etch



Resist B

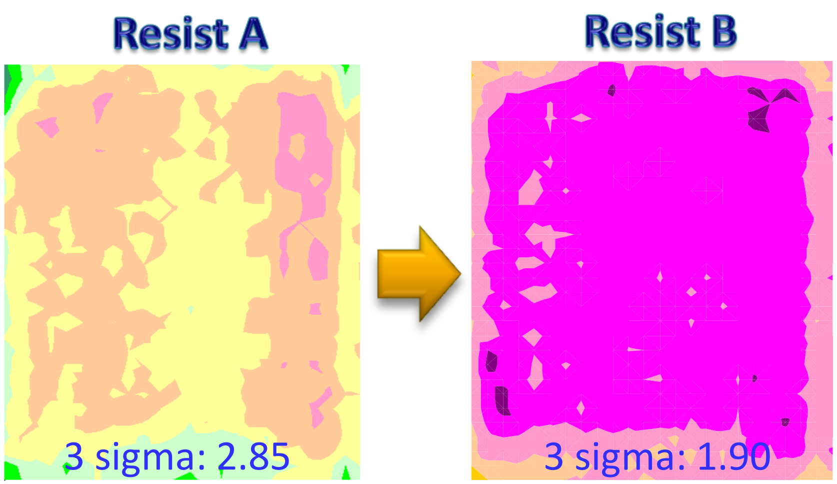
After Litho

After etch (new)

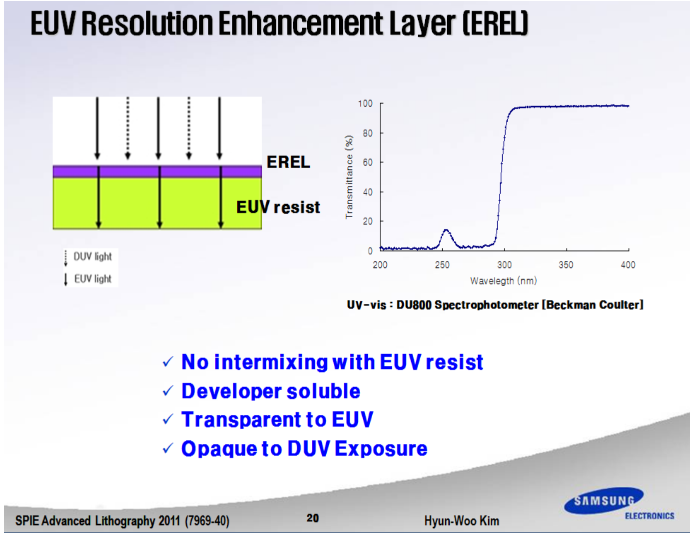


Issue 2: CD variation across a field

- OoB* radiation has impacts on CD variation across a field.
- DUV insensitive resist shows better CD uniformity.
- EREL(EUV topcoat) to filter OoB radiation was developed by Samsung (SPIE 2011).



SPIE 2011



* OoB : Out of Band

2nd generation EUV resist

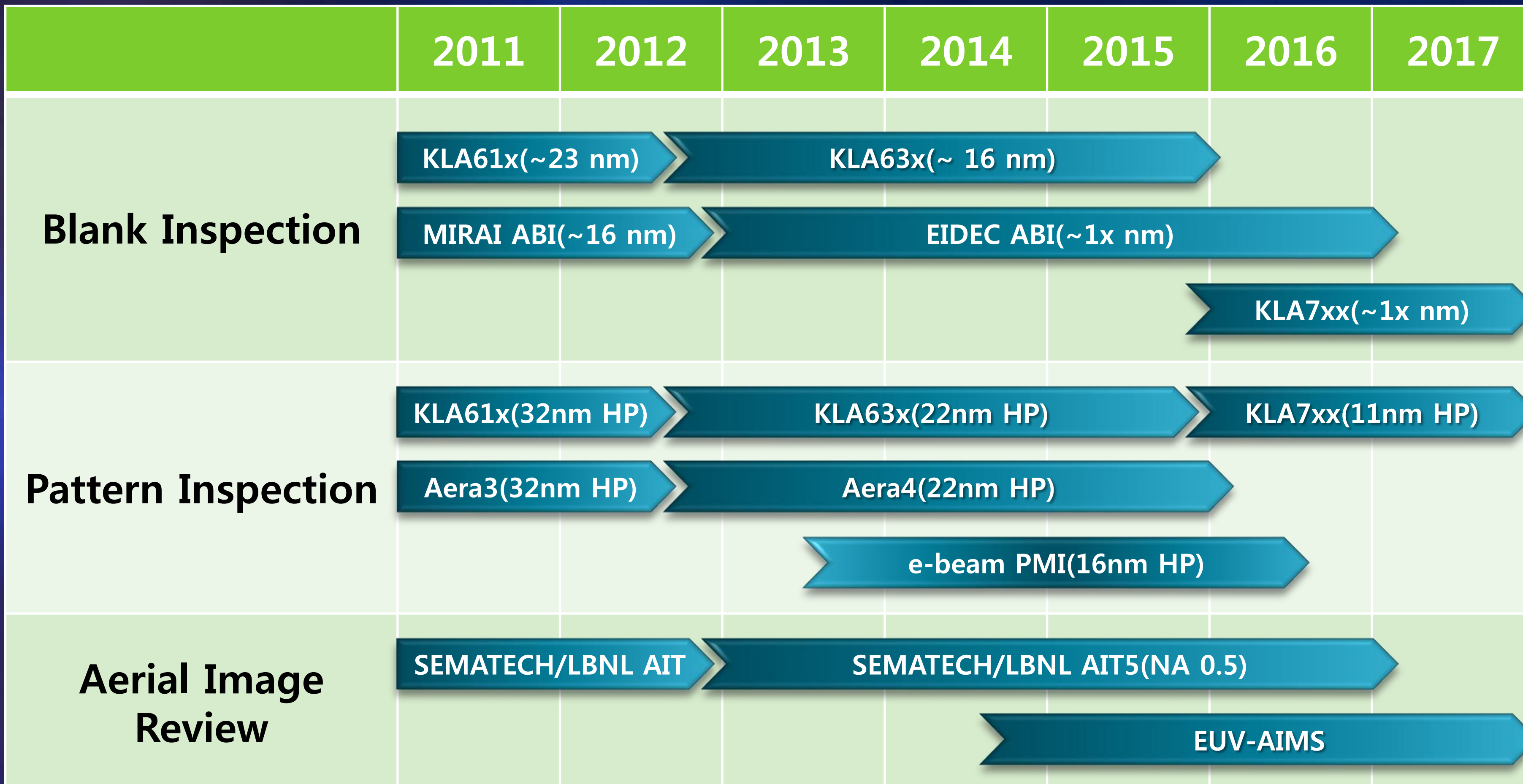
- 20nm HP resolution is required at memory device manufacturer (R&D) from 2012
- More research for 2nd generation EUV resists development is required
- New platform for 2nd generation EUV resist
  - ✓ Drive CAR to have even smaller diffusion length
  - ✓ Upgrade Hf based inorganic resist for mass production

SAMSUNG

Contents

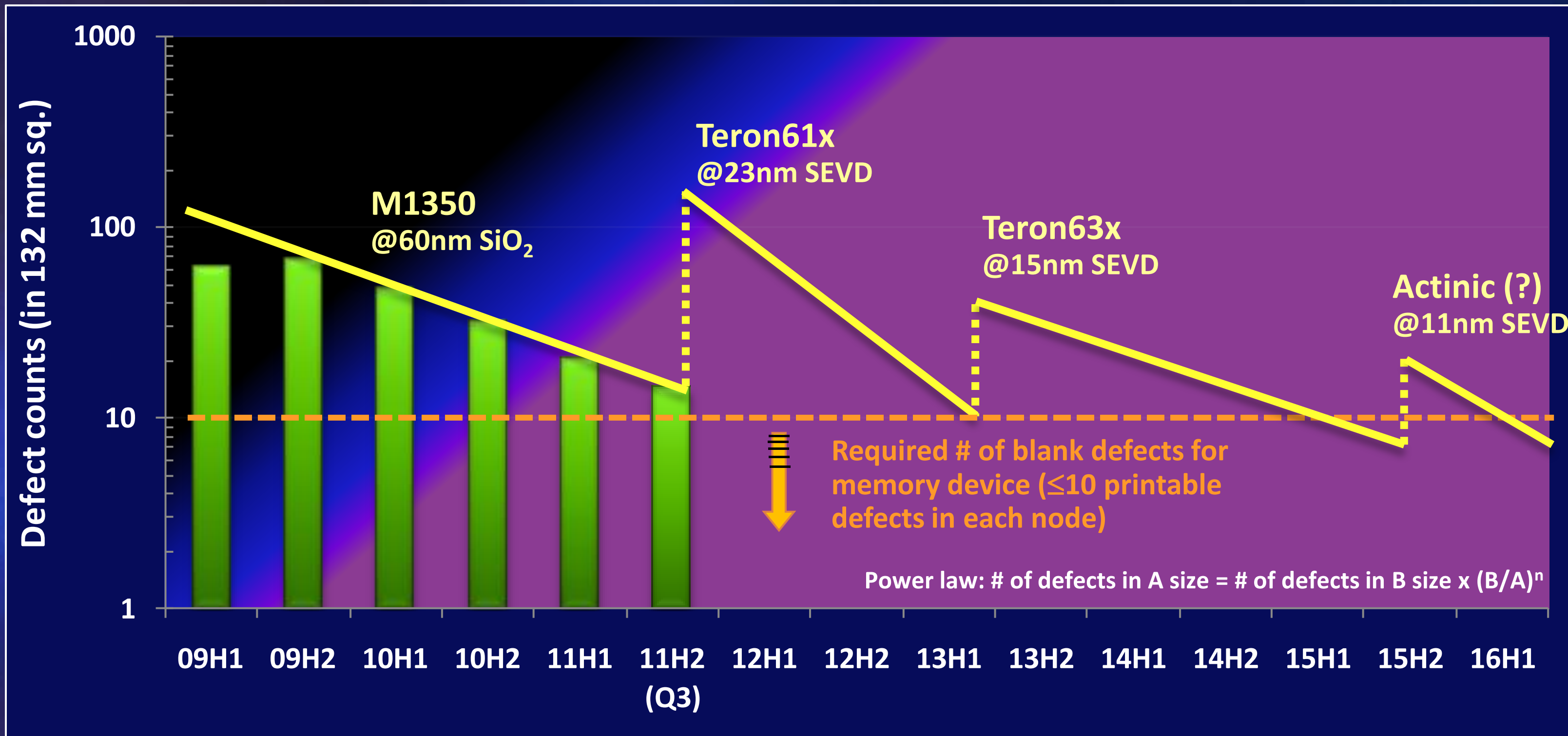
SAMSUNG

EUV mask infra readiness and perspectives



- ✓ **Availability of source for KLA7xx and throughput of e-beam PMI are the biggest challenges.**

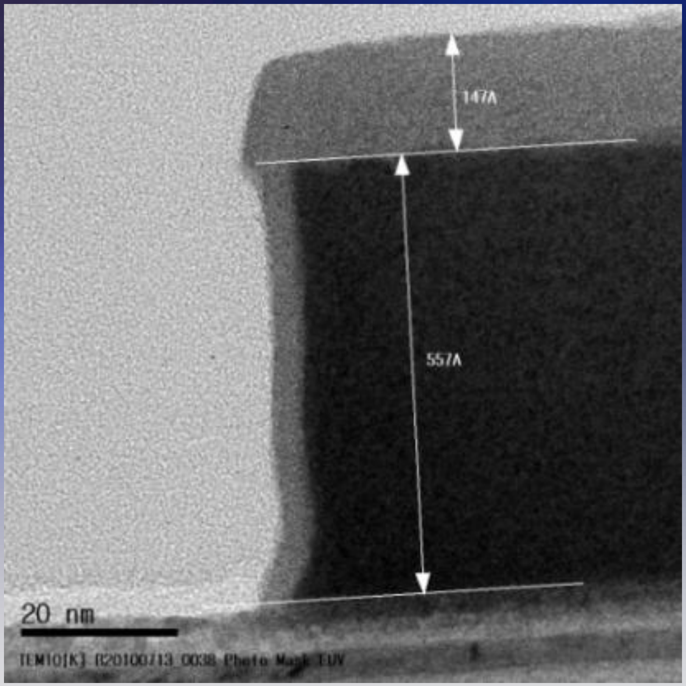
EUV blank defect reduction trend



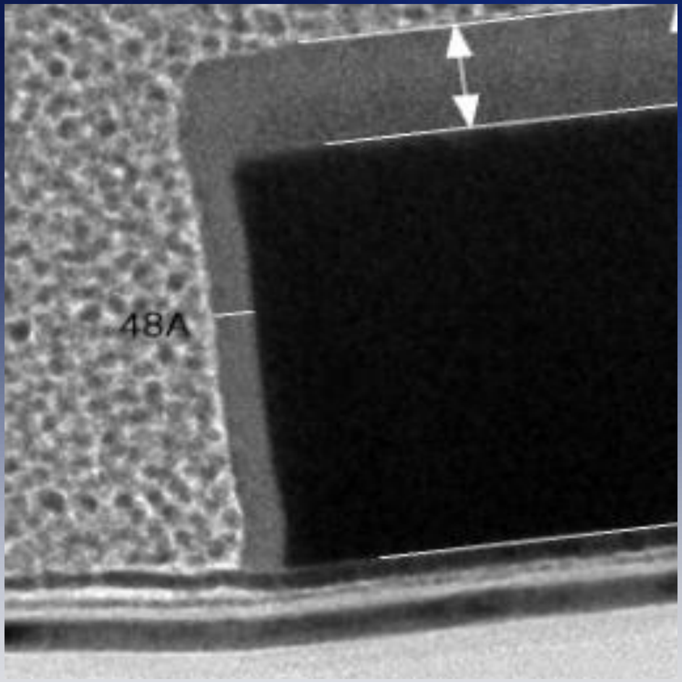
- ✓ Both blank suppliers achieved 1-digit number defects @ 60nm in size for champion blanks
- ✓ ≤ 10 printable defects in each node are the requirements for HVM of memory device (blank defect compensation and repair considered)
- ✓ For logic devices, tighter defect requirements should be applied
- ✓ Corresponding BI tools need to be come into the market on time in each device node.

SAMSUNG

EUV mask patterning capability



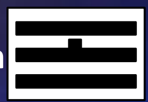
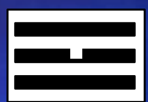
Before improvement



After improvement

✓ **Sidewall angle of ~ 90° is achieved with uniformity of < 1nm**

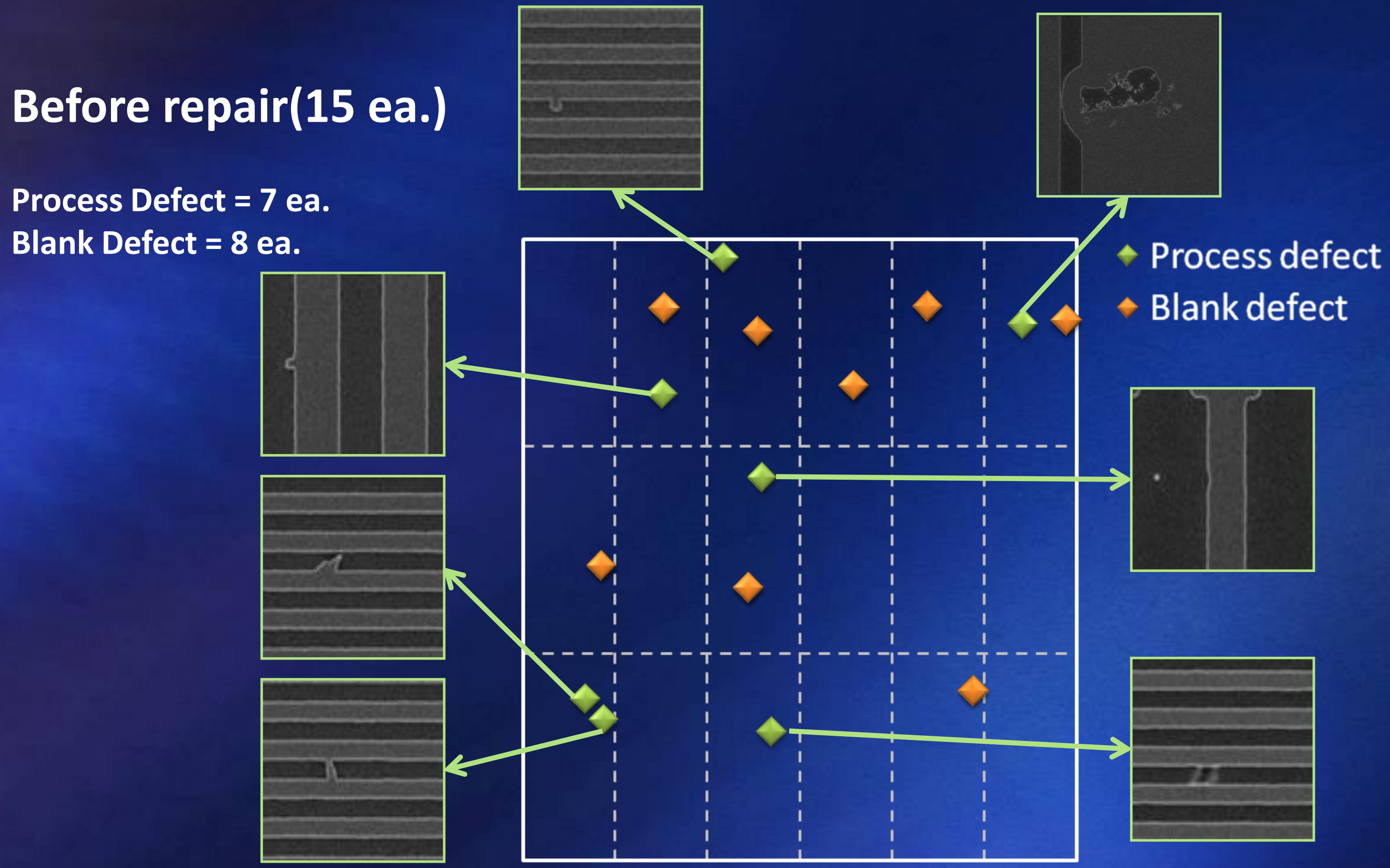
EUV mask inspection capability

30nm L/S		1	2	3	4	5	6	7	8	9	10	11	12
Extrusion 	Printing defect size (nm)	BR	BR	BR	BR	BR	82.1	76.5	59.4	44.8	38.0	32.0	
	Capture rate	100%	100%	92%	100%	88%	100%	100%	100%	100%	100%	60%	
Intrusion 	Printing defect size (nm)	Cut	Cut	Cut	Cut	100	81.8	68.7	56.4	42.0	32.4		
	Capture rate	100%	100%	100%	100%	100%	100%	100%	100%	100%	72%	24%	

24nm L/S		1	2	3	4	5	6	7	8	9	10	11	12
Extrusion 	Printing defect size (nm)	BR	BR	BR	BR	65.3	54.1	49	39.8	32.2	29.2		
	Capture rate	100%	100%	100%	100%	100%	100%	100%	96%	84%			
Intrusion 	Printing defect size (nm)	CUT	CUT	CUT	CUT	68.1	58.6	53.3	41.8	38.2	29.1		
	Capture rate	100%	100%	100%	100%	100%	100%	96%	52%				

- ✓ All printing defects@30nm HP were captured by 193nm-wavelength inspection tool with ~100% of capture rate.
- ✓ Next generation 193nm-wavelength inspection tool is expected to cover beyond 24nm HP.

Challenge for defect-free mask

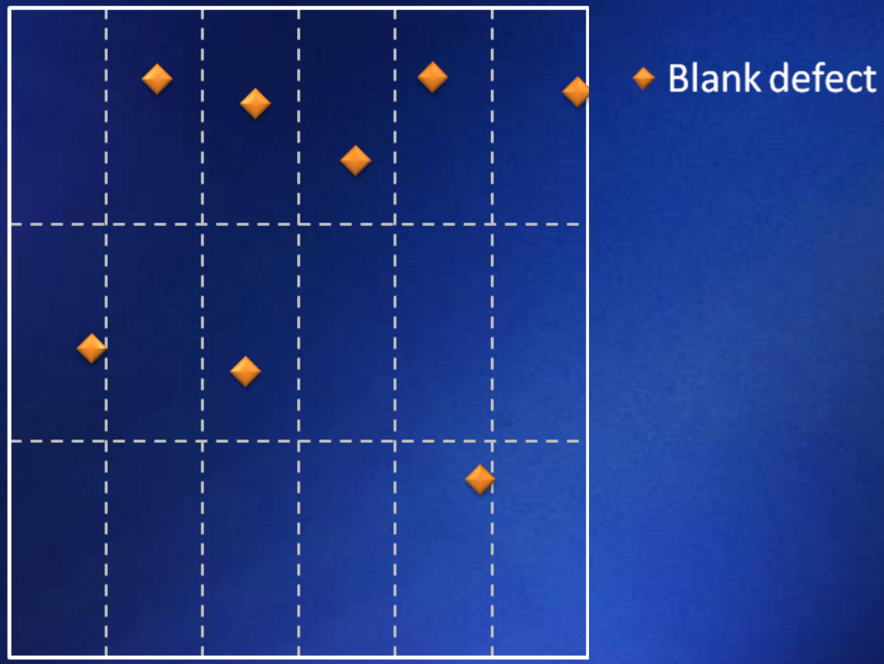


- ✓ All of 7 process defects could be repaired and didn't detected by 193nm-wavelength inspection tool.
- ✓ Blank defects need to be reduced or compensated.

Challenge for defect-free mask

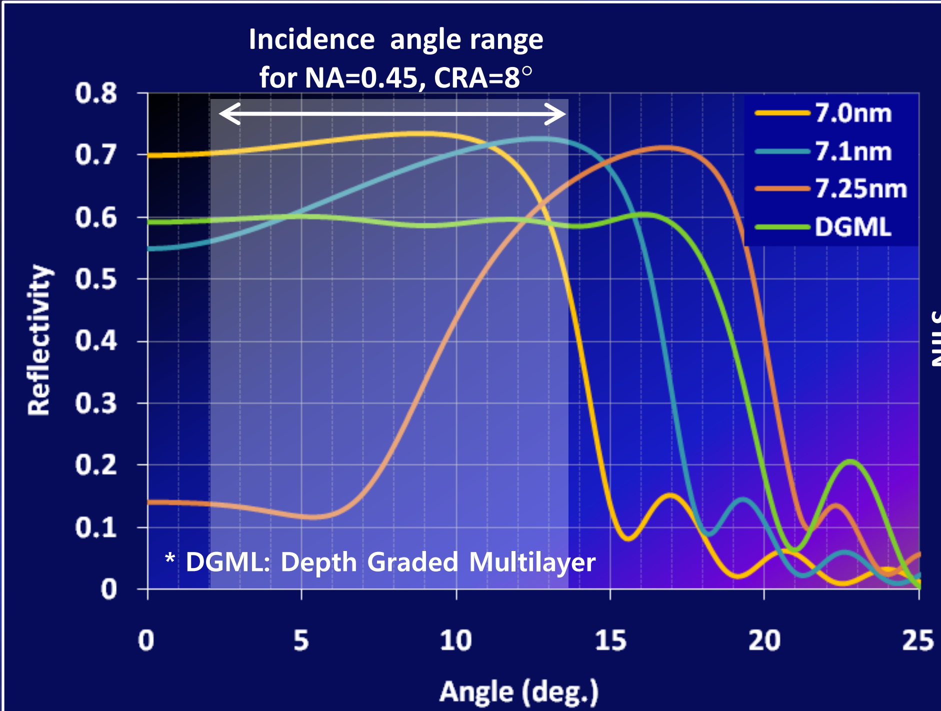
After repair(8 ea.)

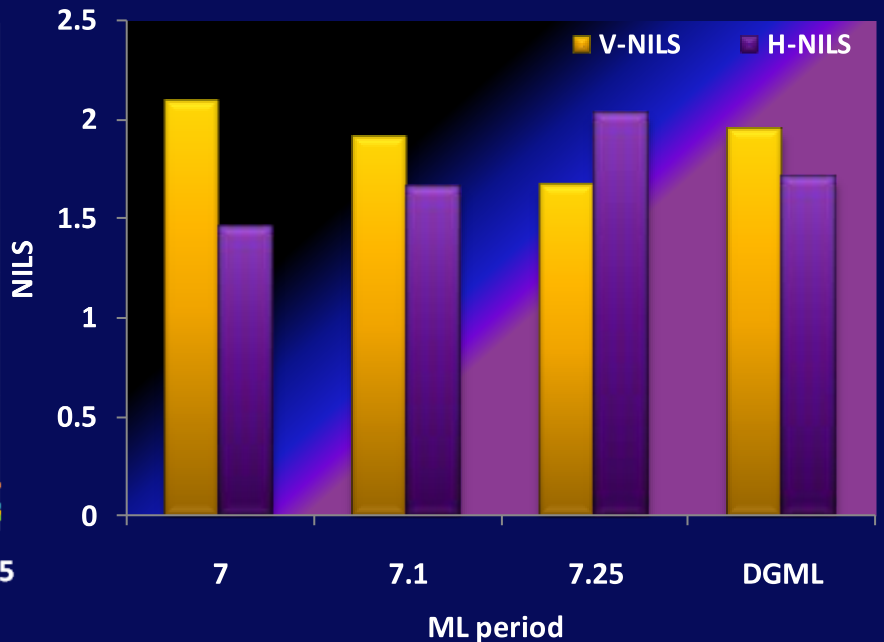
Process Defect = 0 ea.
Blank Defect = 8 ea.



- ✓ **All of 7 process defects could be repaired and didn't detected by 193nm-wavelength inspection tool.**
- ✓ **Blank defects need to be reduced or compensated.**

Imaging issue of EUV mask @NA=0.45 & CRA=8°





- ✓ ML reflectivity shows steep drop within incident angle range for NA=0.45 and CRA* = 8°
- ✓ Uniform reflectivity can be attained by DGML* but NILS is not enough even under strong dipole illumination condition
- ✓ Further breakthrough is needed including new absorber material for EUV single exposure at 11nm HP

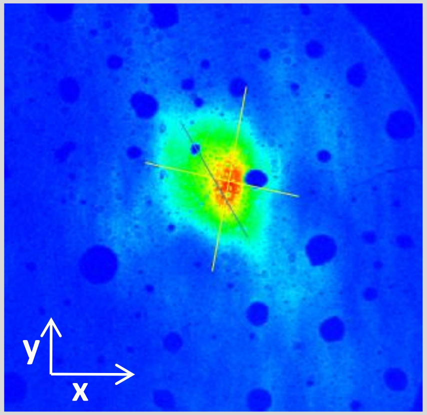
* CRA : Chief Ray Angle, DGML: Depth Graded Multilayer

Other activities

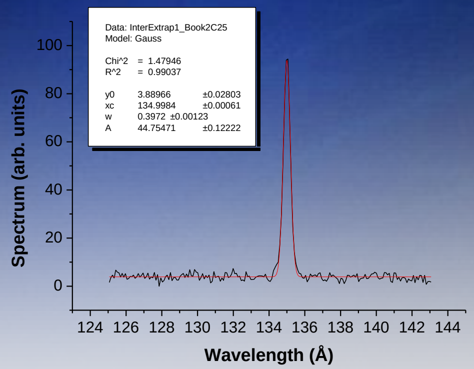
Session9: "Development of coherent EUV source form mask metrology," Dong Gun Lee

❑ Development of high-harmonic EUV source for metrology (w/ FST)

FST's EUV040



Lowest Beam Divergence
(x/y = 0.2/0.25 mrad)



Narrow Spectrum Width
($\lambda/\Delta\lambda$ >280)

- ✓ 48-nW power operating at 1-kHz repetition rate, ~0.2 mrad divergence, and $\lambda/\Delta\lambda$ >280 were attained.
- ✓ High-harmonic EUV source can be applied to stand-alone CSM and other EUV metrology tools

Conclusions

- In the semiconductor industry worldwide, unceasing demand for quicker, faster, and cheaper devices by way of device shrinkage still exists and is also predicted feasible up to sub-10nm design node. As known clearly, we have no alternative but to select EUVL technology for sub-20nm device application or below
- Beyond any doubt the era of EUVL has been already started with a sure technology feasibility. However, more research and development efforts are still required in throughput, defect, overlay, technology extendibility, mask infra structure, etc. to realize for timely mass production. It is expected that only solution to such critical issues can be viable by global collaboration closely aligned with all interested parties
- The final success of EUVL is determined by effective and competitive cost of ownership